AMENDMENTS TO THE CLAIMS

Please amend the claims as reflected in the following claim listing. *(This listing of claims will replace all prior versions and listing of claims in the application.)*

1. **(Previously Presented)** A single transistor ferroelectric memory cell, comprising:

a semiconductor substrate having defined thereon:

a first conductive region of a first conductive type;

a source of a second conductive type defined in said first conductive region, said source sized and configured to comprise the source of the ferroelectric memory cell and the source of an adjacent ferroelectric memory cell; and

a drain also of a second conductive type defined in said first conductive region, said drain being spaced apart from said source such that a channel region comprising a portion of said first conductive region is defined between said source and said drain, said drain also being spaced apart from sources and drains of adjacent ferroelectric memory cells, wherein said drain is not shared with adjacent ferroelectric memory cells;

a gate oxide layer disposed on said semiconductor substrate to cover the entirety of said drain, channel region, and source;

a ferroelectric gate unit positioned on said gate oxide layer such that the ferroelectric gate unit overlies a relatively greater portion of the drain than the source, the ferroelectric gate unit comprising:

a bottom electrode in electrical communication with said drain;

a top electrode;

a ferroelectric layer disposed between said bottom and said top electrode; and

a sealing layer disposed on each side of said ferroelectric gate unit; and

an upper conductive layer disposed on said ferroelectric gate unit and a portion of said gate oxide layer such that said upper conductive layer and said top electrode of said ferroelectric gate unit are in electrical communication.

2. **(Original)** A single transistor ferroelectric memory cell as defined in claim 1, wherein said upper conductive layer comprises polysilicon doped to a conductive state.

3. **(Original)** A single transistor ferroelectric memory cell as defined in claim 1, further comprising a plurality of shallow isolation trenches defined in the semiconductor substrate.

4. **(Original)** A single transistor ferroelectric memory cell as defined in claim 1, further comprising a lower polysilicon layer disposed between said gate oxide layer and said bottom electrode, the lower polysilicon layer doped to a conductive state and having a thickness a thickness of from about 500 to 700 Å.

5. **(Original)** A single transistor ferroelectric memory cell as defined in claim 1, wherein said first conductive region of a first conductive type includes ions implanted therein, said ions taken from the group consisting of B and BF_2.

6. **(Original)** A single transistor ferroelectric memory cell as defined in claim 1, wherein said source and drain regions of a second conductive type include ions implanted therein, said ions taken from the group consisting of P and As.

7. **(Original)** A single transistor ferroelectric memory cell as defined in claim 1, wherein said bottom and top electrode are composed of material taken from the group consisting of Pt, Ir, IrO_2, Ru, and RuO, said bottom and top electrode each having a thickness of about 500 to 1,500 Å.

8. **(Original)** A single transistor ferroelectric memory cell as defined in claim 1, wherein said ferroelectric layer is comprised of material taken from the group consisting of $Pb(Zr, Ti)O_3$, $SrBiTa_2O_9$, $Pb_5Ge_3O_{11}$, and $BaTiO_3$, said ferroelectric layer having a thickness of about 800 to 2,000 Å.

9. **(Original)** A single transistor ferroelectric memory cell as defined in claim 1, wherein said sealing layer comprises material taken from the group consisting of Si_3N_4 and Al_2O_3.

10. **(Original)** A single transistor ferroelectric memory cell as defined in claim 1, wherein the spacing between said source region and said drain region is approximately .18 to .35 μm.

11-21. ~~(Withdrawn)~~ **(Cancelled)**

22. **(Previously Presented)** A ferroelectric memory cell comprising:

a semiconductor substrate having:

a single source that serves as the source for both the ferroelectric memory cell and an adjacent ferroelectric memory cell;

a drain that is spaced apart from the source and from drains and sources of adjacent ferroelectric memory cells, wherein the drain is not shared with the adjacent ferroelectric memory cell; and

a channel defined between the source and the drain;

a gate oxide substantially covering the drain, source, and channel;

a ferroelectric gate unit comprising a top electrode, a layer of ferroelectric material, and a bottom electrode, the ferroelectric gate unit being positioned on the gate oxide, wherein the ferroelectric gate unit substantially overlies the entirety of the drain, and wherein the ferroelectric gate unit overlies only a portion of the source; and

means for controlling the polarization of said layer of ferroelectric material.

23. **(Original)** A ferroelectric memory cell as defined in claim 22, wherein the means for controlling the polarization of said layer of ferroelectric material comprises an electrical connection between said drain and said bottom electrode of said ferroelectric gate unit.

24. **(Previously Presented)** A ferroelectric memory cell as defined in claim 23, wherein the means for controlling the polarization of said layer of ferroelectric material further comprises an upper polysilicon layer deposited on top of said ferroelectric gate unit such that electrical communication is established between said top electrode and said upper polysilicon layer.

25. **(Original)** A ferroelectric memory cell as defined in claim 22, further comprising a lower polysilicon layer deposited between the ferroelectric gate unit and the gate oxide.

26-31. ~~(Withdrawn)~~ **(Cancelled)**

32. **(Previously Presented)** A single transistor ferroelectric memory cell as defined in claim 1, wherein the ferroelectric gate unit is positioned such that asymmetric source and drain regions are defined.

33. **(Previously Presented)** A ferroelectric memory cell, comprising:

a semiconductor substrate having:

a source that serves both as the source for the ferroelectric memory cell and the source for an adjacent memory cell;

a drain in a spaced apart configuration with respect to the source and drains and sources of adjacent ferroelectric memory cells, wherein the drain is not included as a component of the adjacent ferroelectric memory cell; and

a channel;

a gate oxide substantially covering the drain, source, and channel;

a ferroelectric gate unit positioned on said gate oxide layer, the ferroelectric gate unit asymmetrically overlying the drain with respect to the source, the ferroelectric gate unit comprising:

a bottom electrode in electrical communication with said drain;

a top electrode;

a ferroelectric layer disposed between said bottom and said top electrode; and

a sealing layer disposed on each side of said ferroelectric gate unit; and

an upper conductive layer disposed on said ferroelectric gate unit and a portion of said gate oxide layer such that said upper conductive layer and said top electrode of said ferroelectric gate unit are in electrical communication.

34. **(Previously Presented)** A ferroelectric memory cell as defined in claim 33, wherein the ferroelectric gate unit is positioned such that it overlies the entirety of the drain.

35. **(Previously Presented)** A ferroelectric memory cell array, comprising:

first and second ferroelectric memory cells that are positioned adjacent one another on a semiconductor substrate, the first ferroelectric memory cell including:

a source defined in the semiconductor substrate that is configured for use as the source for both the first and second ferroelectric memory cells;

a first drain defined in the semiconductor substrate in a spaced apart configuration with respect to both a second drain of the second ferroelectric memory cell and the source, wherein the first drain is not included as a component of the second ferroelectric memory cell;

a channel defined in the semiconductor substrate;

a gate oxide substantially covering the first drain, source, and channel;

a ferroelectric gate unit positioned on said gate oxide layer, the ferroelectric gate unit asymmetrically overlying the first drain with respect to the source, the ferroelectric gate unit comprising:

a bottom electrode in electrical communication with the first drain;

a top electrode;

a ferroelectric layer disposed between said bottom and said top electrode; and

a sealing layer disposed on each side of said ferroelectric gate unit; and

an upper conductive layer disposed on said ferroelectric gate unit and a portion of said gate oxide layer such that said upper conductive layer and said top electrode of said ferroelectric gate unit are in electrical communication.

36. **(Previously Presented)** The ferroelectric memory cell array as defined in claim 35, wherein the second ferroelectric memory cell includes the source and the second drain, the second drain being in a spaced apart configuration with respect to the first drain and the source, and wherein the second drain is not included as a component of the first ferroelectric memory cell.